IN THE SPECIFICATION

Please replace paragraph 0085 with the following amended version:

--Referring now to FIG. 9, a block diagram of a PCI Express packet 900 is shown. The details of each of the blocks in the PCI Express packet 900 are thoroughly described in the PCI Express Base specification 1.0a ~~(a specification that does not include provisions for sharing I/O)~~ published by www.pcisig.com, which is incorporated herein by reference for all purposes. Additional information may be found in the texts referenced above with respect to FIG. 2C.—

Please replace paragraph 0131 with the following amended version:

--FIG. 19 is an architectural diagram illustrating packet flow from three root complexes to three different shared I/O fabrics through a shared I/O switch according to the present invention. In one embodiment, the shared I/O fabric utilizes a PCI Express Architecture which is a base specification 1.0 that does not include provisions for sharing I/O. FIG. 19 illustrates an environment 1900 that includes a number of root complexes (or OS Domains) 1902, 1904, 1906 coupled to a shared I/O switch 1910 using a non- shared load/store fabric 1908 such as PCI Express. The shared I/O switch is coupled to three shared I/O controllers, including an Ethernet controller 1912, a Fiber Channel controller 1914 and an Other controller 1916. Each of these controllers 1912-1916 are coupled to their associated fabrics 1920, 1922, 1924, respectively.--